Si3000PPT-EVB

EVALUATION BOARD FOR THE Si3000 WITH THE PARALLEL PORT INTERFACE

Description

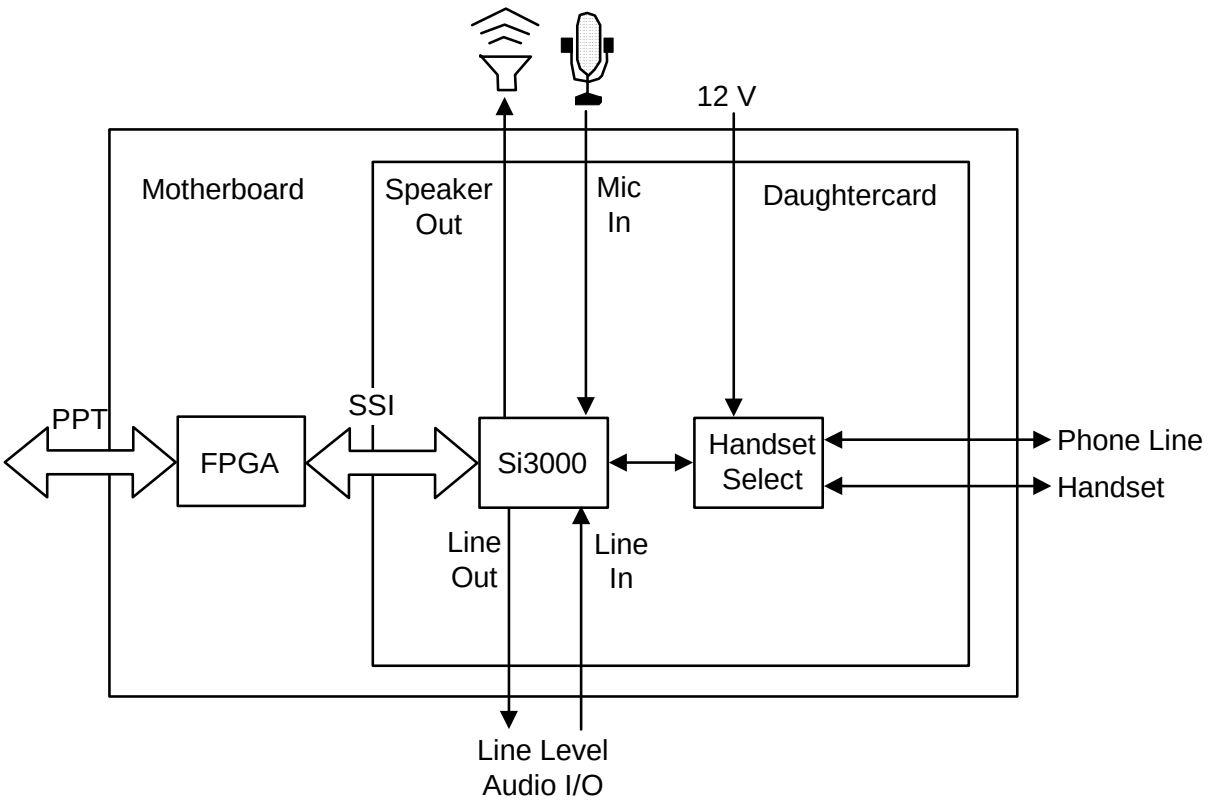
The Si3000PPT-EVB provides the audio system engineer an easy way to evaluate the functionality of Silicon Laboratories' Si3000 voice band codec solution. The Si3000 chipset can be easily controlled from a PC using the supplied application software (requires Si30xxPPT software Rev 2.1 or above and FPGA Rev 2.1 or above).

Features

The Si3000PPT-EVB includes the following:

- Ability to read and write registers
- DAC waveform generation from a series of standard waveforms or from a .wav file
- ADC data capture and display in either time or frequency domain
- Recommended layout for key components
- Daisy-chain support when used with Si30xx (Si3034, Si3035, Si3044, or Si3056) products
- RJ-11 Interface to Handset
- RJ-11 Connection to Phone Line and Modem
- Microphone, Speaker Interfaces
- Line In, Line out Interfaces

Functional Block Diagram



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Functional Description

The Si3000PPT-EVB provides the audio system engineer an easy way to evaluate the Si3000 voice band codec solution.

The Si3000PPT-EVB also supports the connection of multiple devices on an SSI interface. The evaluation board provides a straightforward means of evaluating this feature.

The evaluation board consists of the Si30xxPPT-EVB motherboard and the Si3000DC_EVB daughter card. A custom ribbon cable is also provided to connect to the parallel port of a PC. Contact a Silicon Laboratories representative for more information.

In this document, the Si3000DC-EVB is occasionally referred to as the “daughter card” and the Si30xxPPT-EVB as the “motherboard”. The Si3000PPT-EVB refers to the system which consists of both the “motherboard” and “daughter card”.

Motherboard–Daughter Card Connection

The Si3000DC-EVB connects to the Si30xxPPT-EVB through two sockets: JP1 and JP2. JP1 is a 3x8 socket connection to the digital signals of the DSP-side chip. In addition, a 3.3 V regulated supply is routed to this socket and supplies the power to the digital-side device. JP1 of the daughter card connects to JP2 of the Si30xxPPT-EVB. JP2 is a 2x5 socket connection from the TIP and RING and chassis ground of the line interface to the line-side device. JP2 of the Si3000DC-EVB connects to JP1 of the Si30xx PPT EVB.

Power Supply

Power is supplied to the EVB by means of J3 or J4. J3 is a euroblock header that allows for connection to a bench power supply. J4 is a 2.1 mm power jack that allows the use of a wall transformer. A 9 V supply/ 300 mA is typically used, but the onboard voltage regulator also works with a dc voltage between 7.5 V and 20 V. A diode bridge is used to correct polarity. The on-board regulator, U7, provides 5 V to the call progress circuit, the on-board oscillator, and other boards daisy chained to the Si30xxPPT-EVB. This 5 V is further regulated to 3.3 V to power the daughter card and the input/output ports of the FPGA. A third regulator provides 2.5 V for the core voltage of the FPGA.

Clock Generation

The Si3000 requires an MCLK input. An on-board oscillator (Y1) is used by the FPGA to clock all the subsystems as well as generate and provide the master clock to the Si3000. The FPGA is designed to use a 18.432 MHz oscillator (included with the board).

Optional Call Progress Speaker

This feature is not utilized by the Si3000

Reset Circuit

The Si3000 requires an active low pulse on RESET following powerup and whenever all registers need to be reset. For development purposes, the Si3000PPT-EVB includes a reset push button, SW1, that is used by the FPGA to generate the reset pulse of the Si3000.

If multiple boards are cascaded together, the reset signal should be generated by the master board. Using the SW1 pushbutton on slave boards does not reset that slave board.

Serial Modes

The Si3000 supports several different serial modes for a glueless interface to many standard DSP and ASIC serial ports. The serial mode of the Si3000 can be selected by JP3 and JP4 on the motherboard.

Line Connection

The Si3000PPT-EVB has a physical interfaces designed to connect to the phone line. It is on the daughter card. These interfaces are equivalent and interchangeable. When using the Si3000PPT-EVB in slave mode, one of the line interfaces is used to connect to the phone line, while the other line interface is used to connect to the Master Board Modem Line Interface. This way, both the Si3000PPT-EVB and Si30xxPPT-EVB gain access to the phone line without requiring an external phone splitter.

Handset Interface

The Si3000PPT-EVB includes a handset interface. This interface is located on the daughter card J1 connector pins 9 and 10.

A handset can connect directly to the phone line or the the Si3000 device. The target system is expected to control the DPDT relay to select the handset connection. When the handset is connected to the Si3000, both the Si3000 and handset are disconnected from the phone line. In this case, the Si3000PPT-EVB supplies dc power to the handset through an external 12 Vdc bench supply. The euroblock header, J6, on the daughter card is provided for this connection. 24.5 mA of DC loop current is supplied to the handset.

In a voice modem application, the Si3000PPT-EVB is configured in the slave mode, with an Si30xxPPT-EVB acting as the master board. When this system is in the on-hook state, either the Si30xx or the handset can respond to the phone ring and place the system in the off-hook state.

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If the system software chooses to allow the Si30xx EVB to go off hook, the handset is excluded from the phone loop and is connected directly to the Si3000 EVB. Voice traffic is handled by the Si3000 and system software is responsible for creating a virtual voice connection between the handset and the phone system through the Si3000 and Si30xx devices.

Microphone Interface

A standard 3.5 mm mini-phono connector located on the daughter card connector J2 is used to provide an interface from an external microphone to the Si3000. The input impedance to MIC input of the Si3000 is at least 10 kW. The Si3000 has a programmable pre-amplification to support many input line levels.

If Jumper JP3 on the daughter card is populated, the microphone can be powered directly from the Si3000 MBIAS output. The MBIAS output provides a typical voltage of 2.5 V and can supply up to 5 mA, programmable through an external resistor. For applications that cannot be met by the Si3000's MBIAS output, the jumper may be removed and an external biasing voltage can be applied to the microphone.

Speaker Interface

A standard 3.5 mm mini-phone connector is located on the daughter card connector J3. The Si3000 SPKRR and SPKRL outputs are designed to drive 60 W loads directly. To drive a 32 W headset, an external series resistor (30 W) is needed. Driving a 32 W headset directly may result in reduced THD and Dynamic Range performance. The maximum voltage swing is 1 Vrms for either the left or right speaker drivers. The Si3000 speaker outputs have programmable analog attenuation.

Line Input Interface

A standard RCA jack on the daughter card connector J5 is used to provide the line-level audio inputs to the Si3000. The Si3000 has a programmable pre-amplifier. The input impedance of the LINEI is at least 10 kΩ. The Si3000 supports multiple levels of pre-amplification to support various line-levels.

Line Output Interface

A standard RCA jack on the daughter card connector J4 is used to provide the line-level audio outputs from the Si3000. The Si3000 line output gain is programmable. The maximum output voltage is 1 Vrms.

PC Parallel Port

JP13 connects through the Silicon Labs custom ribbon cable to the parallel port of the PC. The parallel port connection allows the designer to read and write the Si3000 register using the evaluation software included with the Si3000PPT-EVB.

Configuring the Si3000PPT-EVB

The S3000PPT-EVB is used to interface the Si3000 audio codec to a PC or other audio system for easy evaluation. It uses an FPGA to translate the parallel port interface to the SSI bus to communicate to the Si3000. The audio data and control data are communicated from the controlling PC using the aforementioned software. This mode allows the user to evaluate the Si3000 without any lab equipment other than a PC.

When in mode 0, the negative edge of FSYNC indicates the starting of the frame, and FSYNC is low until the end of data transfer. By selecting mode 1 operation, the rising edge of FSYNC indicates the start of the frame but is only high for one cycle. To evaluate the Si3000's multiple device operation, chain the slave boards with JP3 and JP4 on the moterboard to set to Mode 2. See Table 1 for a description of these operating modes.

Table 1. Mode Configuration

Mode	M1	M2	Description
0	0	0	FSYNC frames data
1	0	1	FSYNC pulse starts data frame
2	1	0	Slave mode
3	1	1	Reserved

The evaluation board has the ability to interface in two different modes of the SSI bus: 5-bit address space operation is used for the Si3000/34/35/44, and 7-bit address space operation is used for the Si3056. The on-board FPGA will auto-detect the chip and set the appropreate registers.

Evaluation Software

The Si3000PPT-EVB includes an easy-to-use graphical interface for controlling the evaluation platform. The software is called Si30xxPPT evaluation software. This software allows the system designer to characterize the Si3000 voice band codec performance without constructing any custom hardware. The evaluation software includes the following features:

- Ability to read and write the Si3000 registers using the SSI bus
- DAC waveform generation from a series of standard waveforms or from a .wav file
- ADC data capture and display in either time or frequency domain using the SSI bus
- Daisy-chain support
- Transmit and receive path attenuation and gain settings

PC System Requirements

The application software for the Si30xxPPT-EVB has the following system requirements:

- Windows98 or Windows2000
- Available parallel port
- EPP or ECP parallel port mode for Windows 98
- EPP parallel port mode for Windows 2000
- 450 MHz Pentium II or greater recommended
- 64 MB of memory or greater recommended

Installation

The supplied CD contains the Si30xxPPT-EVB windows driver files as well as a setup utility for installing the evaluation software.

To install the Si30xxPPT-EVB software, run the installation program on the “Silicon Laboratories Wireline Software CD.” The path for the installation program is Si30xx Evaluation Software\setup.exe. The installer guides the user through the installation process for Si30xxPPT-EVB.exe and the LabVIEW Run-Time engine.

Using the Si3000PPT-EVB Application Software

A shortcut for starting the application software that controls the Si3000PPT-EVB is installed in the Windows Start Menu under the Programs folder in the “Si30xx Evaluation Software” folder.

Application Menus

Three pulldown menus are used to configure the operation of the software:

- Run:
  - Exit: Stops the program
  - Save: Stores the audio waveform into .wav files
- Configure:
  - Configure Device: Display hardware status and user configuration. User can set advanced software options.
  - Reset Device: Resets device and executes basic initialization sequences.
- Design Tool
  - Register Map: Displays register map of the device
  - Signal Flow Diagram: Displays signal flow diagram of the device.
  - Transhybrid Loss Calculation: Calculate transhybrid loss over frequency
  - Ringing: Helps user program ring validation registers.
- Help: Displays information about the evaluation board

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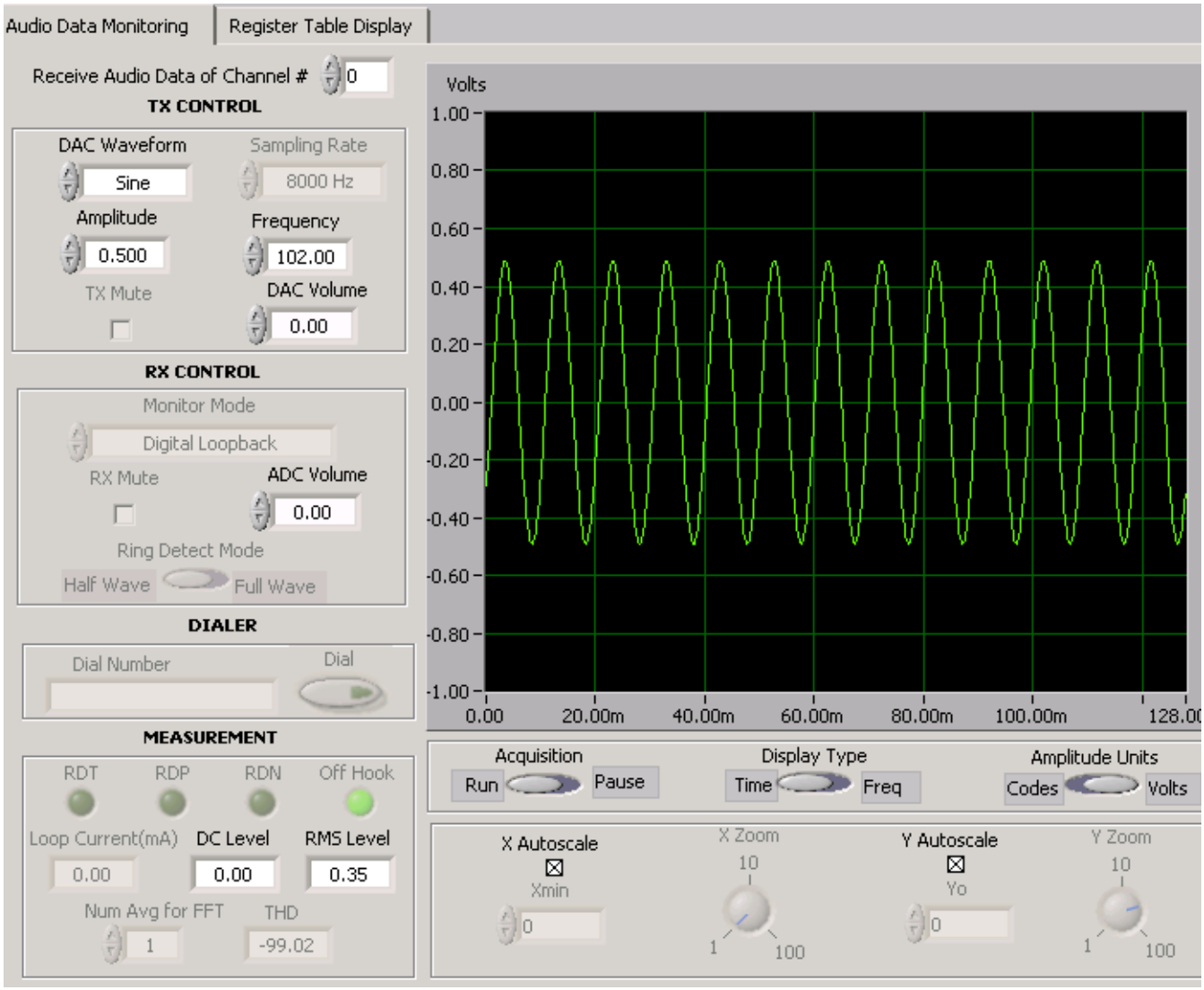


Figure 1. Si30xxPPT-EVB Evaluation Software in the Audio Data Monitoring View

Audio Data Monitoring View

The audio data monitoring view is discussed in the following sections.

Receive Audio Data of Channel#

Allows selection of channel to control and view. The Audio Data Monitoring view allows the generation of DAC data and the capture and display of ADC data. Operation of the front panel in Line Monitoring view is detailed in the following list. See Figure 1.

TX Control

- DAC Waveform: Selects the waveform to be generated by the DAC. The waveform types are as follows: dc, Sine, Square, Ramp, and .wav file.
- TX Gain (dB): Selects the transmit path gain/ attenuation.
- TX Mute: This function is not availabe on the Si3000PPT-EVB
- Sampling Rate: This function is not availabe on the Si3000PPT-EVB
- Amplitude: Sets the amplitude of the DAC waveform in either volts or the units of DAC codes. The units are determined by the Amplitude Units control.
- Frequency: Selects the frequency (Hz) of the waveform to generate. The actual waveform frequency may vary slightly from the entered value. This variation is due to the requirement to fit an integer number of samples into the transmit buffer. The control is updated to reflect the actual waveform frequency generated. The equation for calculating

the frequency of the waveform is as follows: Actual Frequency = round ((Waveform Frequency/n DAC Sample Rate) x BufferSize) x (DAC Sample Rate/BufferSize)

RX Control

- Monitor Mode: This function is not availabe on the Si3000PPT-EVB
- RX Gain/Attn (dB): Selects the receive path gain/ attenuation.
- RX Mute: This function is not availabe on the Si3000PPT-EVB
- Ring Detect Mode: This function is not availabe on the Si3000PPT-EVB

Dialer

- Dial Number: This function is not availabe on the Si3000PPT-EVB
- Dial: This function is not availabe on the Si3000PPT-EVB

Measurement

- Loop Current: This function is not availabe on the Si3000PPT-EVB
- Ring Detect Bits: This function is not availabe on the Si3000PPT-EVB
- Off-Hook: This function is not availabe on the Si3000PPT-EVB
- DC Level/SINAD: Displays either the dc level of the time domain waveform or the SINAD of the frequency domain waveform.
- RMS Level/Frequency: Displays either the RMS level of the time domain waveform or the frequency of the largest peak in the frequency domain waveform.
- Num Avg for FFT: When in FFT display, the software automatically averages waveforms. This panel selects the number of averages to take.

Wave Display Controls

- Display Type: Selects how the ADC data is displayed on the Waveform Graph (time or frequency domain).
- Amplitude Units: Sets the amplitude units for the Waveform Graph and Amplitude control to either volts or codes.
- Acquisition: Used to run or pause the CODEC data stream. Upon pausing the acquisition of the data, it displays measurement values regardless of the status of “display measurement” under the configure menu.
- X Autoscale: Automatically scales the X-axis of the graph to fit the entire waveform.
- Y Autoscale: Automatically scales the Y-axis to fit the entire vertical range of the waveform.
- Xmin: Sets the origin of the X-axis when the X Autoscale is disabled.
- X Zoom: Used to zoom a portion of the displayed waveform when X Autoscale is disabled. The waveform starts at Xmin and 1/X Zoom of the total waveform is displayed.
- Yo: Sets the origin of the Y-axis when Y Autoscale is disabled. Half of the waveform is displayed above Yo, and half is displayed below Yo.

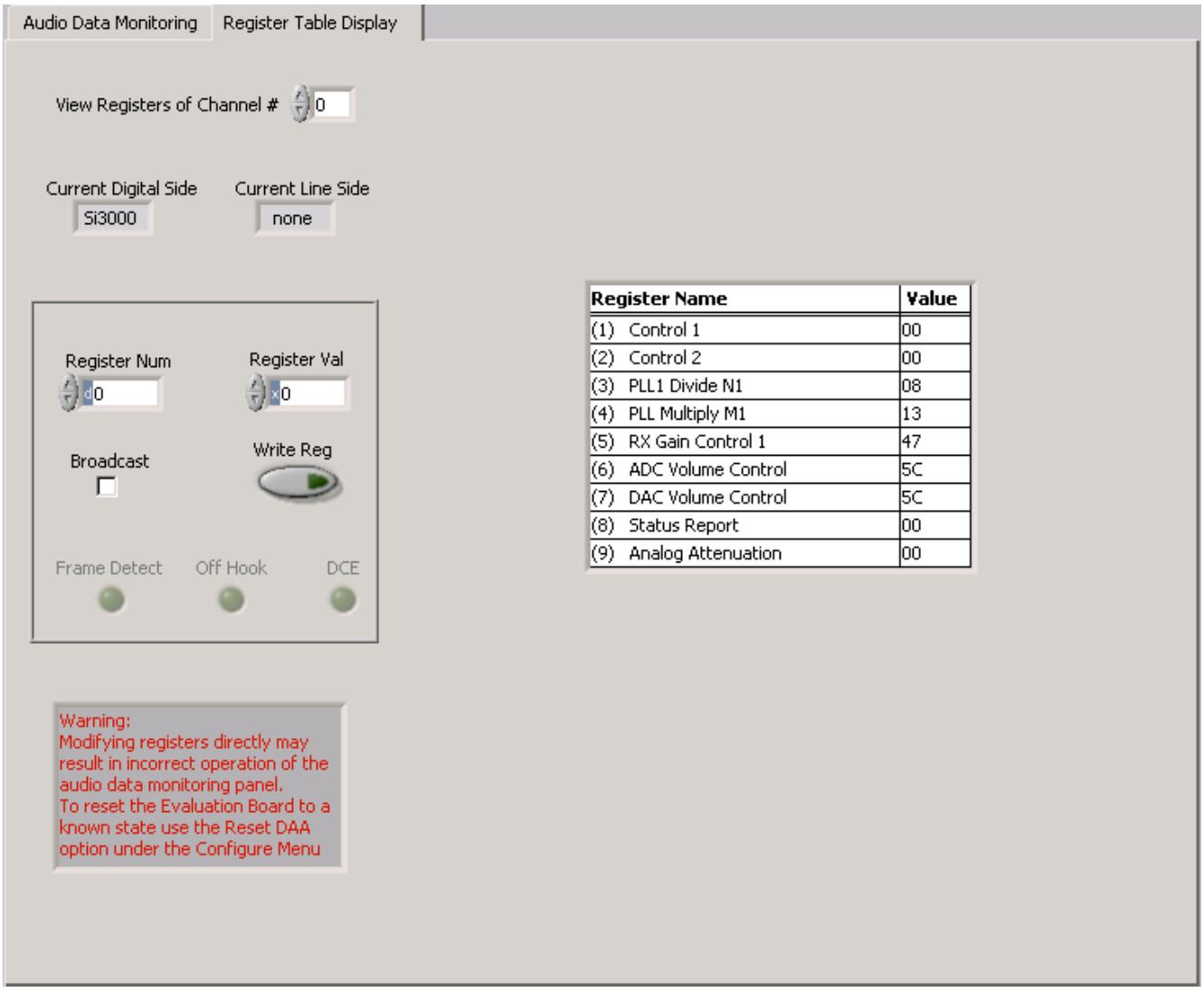


Figure 2. Si30xxPPT-EVB Evaluation software in the Register Monitoring View

Register Table Display View

The Register view allows the Si3000 registers to be read or written. The user interface for the Si3000 Register view is shown in Figure 2. Operation of the front panel in the Si3000 Register view is detailed in the following list:

- Table: This table displays the contents of the Si3000 voice band codec registers in realtime.
- Current Digital Side: Displays the DSP side device on the daughter card.
- Current Linde Side: Displays the Line side device on the daughter card.
- Register Num: The Si3000 register number to write (in decimal).
- Register Val: The contents to write to the register selected by the Register Num control (in hexadecimal).
- Write Regs: Causes the contents of the Register Val control to be written to the Register Num register.
- Broadcast: Write to all the devices in the chain.
- FDT: This function is not availabe on the Si3000PPT-EVB
- Off-Hook: This function is not availabe on the Si3000PPT-EVB
- DCE: This function is not availabe on the Si3000PPT-EVB

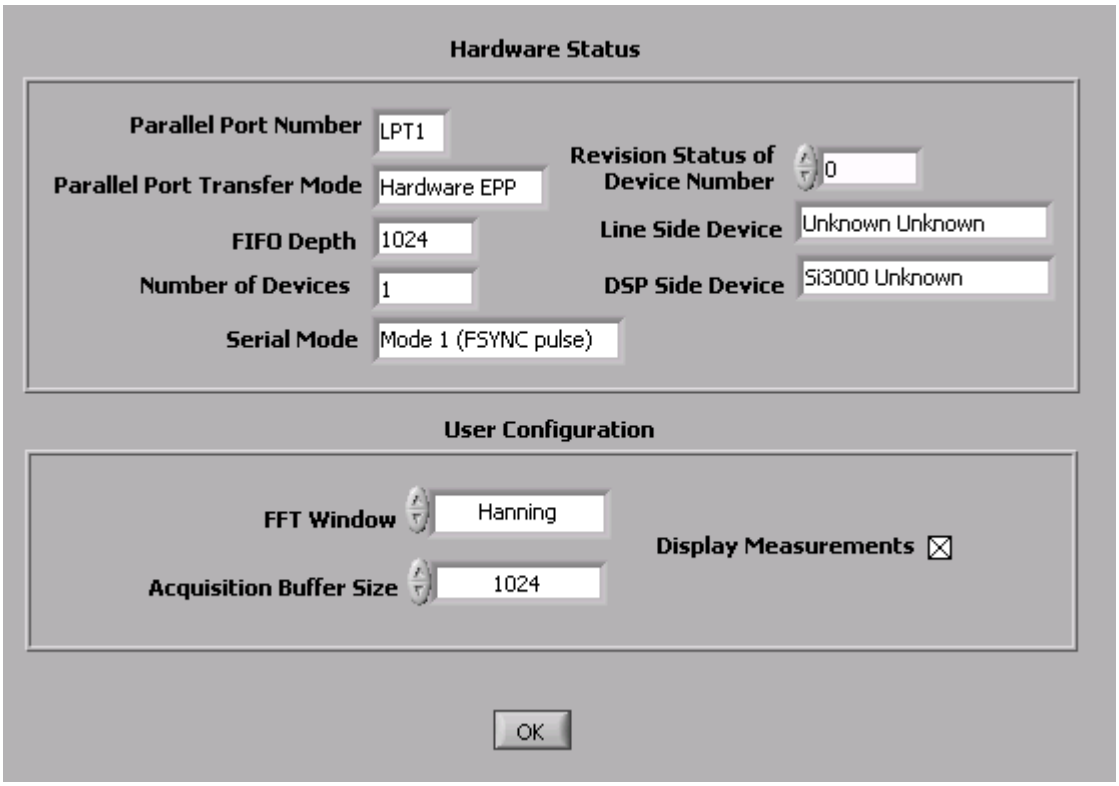


Figure 3. Configuration Device Panel

Advanced Configuration

Advanced configuration of the application software is accomplished by using the “Configure Device” selection in the “Configure” menu. The configuration panel is shown in Figure 3. The panel contents are detailed in the following list:

- FFT Window: The FFT window applied to the time domain data before calculating the FFT.
- Acquisition Buffer Size: This is the size of the buffer, in samples, that is acquired and displayed on the Line Monitoring mode waveform graph. The buffer size can be set between 1024 and 65536 samples in increments of 512 samples.
- Display Measurement: Takes realtime measurements of audio waveform.

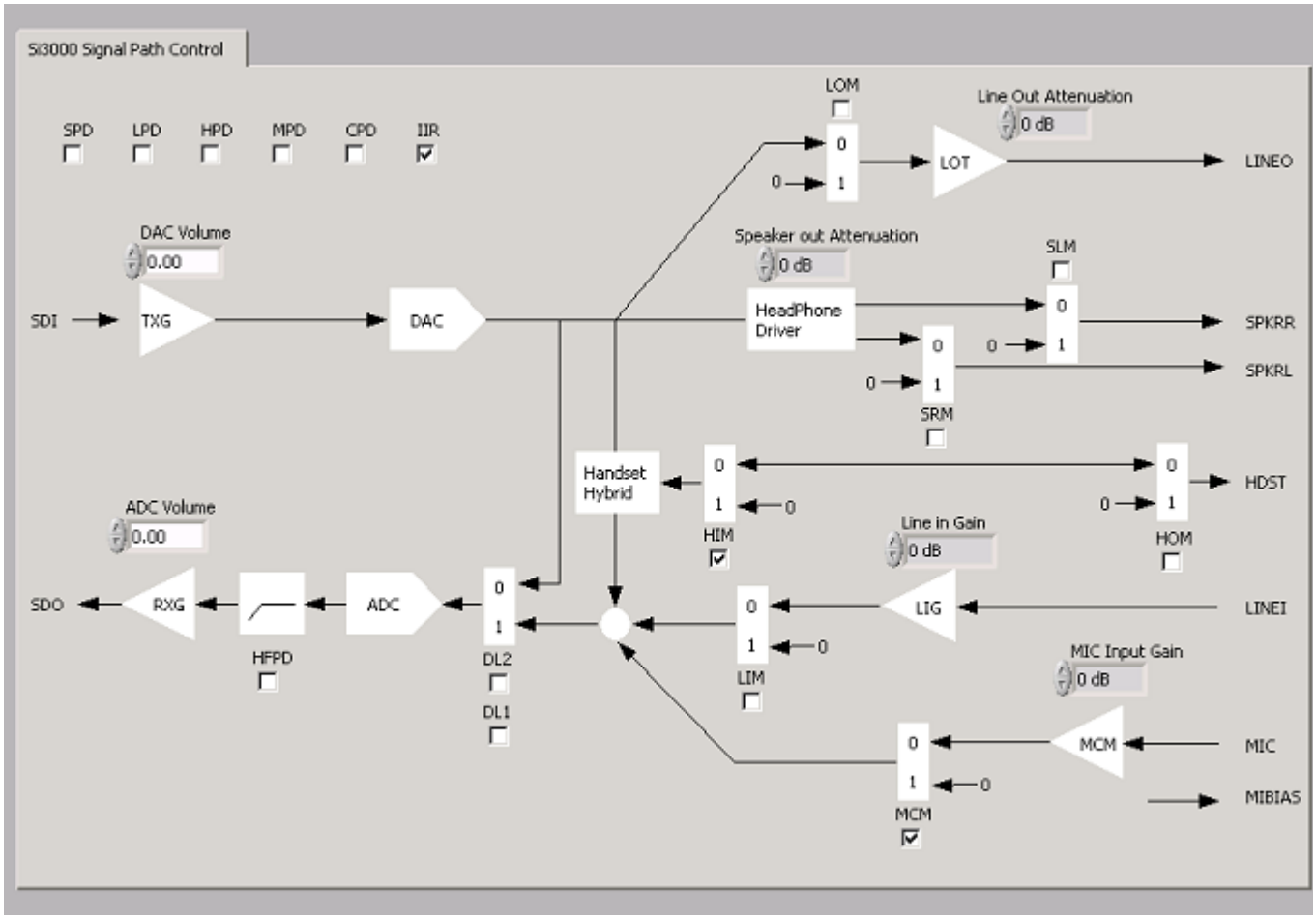


Figure 4. Si3000 Signal Flow Diagram

Signal Flow Diagrams

The signal flow diagrams of the Si30xx evaluation software for the Si3000 device shown in Figure 4 assist users with programming the Si3000.

- SPD: Turns on/off the SPD bit on Register 1, bit 4.
- LPD: Turns on/off the LPD bit on Register 1, bit 3.
- HPD: Turns on/off the HPD bit on Register 1, bit 2.
- MPD: Turns on/off the MPD bit on Register 1, bit 1.
- CPD: Turns on/off the CPD bit on Register 1, bit 0.
- HPFD: Turns on/off the HPFD bit on Register 2, bit 4.
- DLL1: Turns on/off the DLL1 bit on Register 2, bit 2.
- DLL2: Turns on/off the DLL2 bit on Register 2, bit 1.
- Line in Gain: Writes to LIG on Register 2.
- LIM: Turns on/off the LIM bit on Register 2, bit 5.
- MIC Input Gain: Writes to MCG on Register 2.
- MCM: Turns on/off the MCM bit on Register 2, bit 2.
- HIM: Turns on/off the HIM bit on Register 2, bit 1.
- IIR: Turns on/off the IIR bit on Register 2, bit 0.
- ADC Volume: Writes to RXG on Register 6.
- LOM: Turns on/off the LOM bit on Register 6, bit 1.
- HOM: Turns on/off the HOM bit on Register 6, bit 0.
- DAC Volume: Writes to TXG on Register 7.
- SLM: Turns on/off the SLM bit on Register 7, bit 1.
- SRM: Truns on/off the SRM bit on Register 7, bit 0.
- Line Out Attenuation: Writes to LOT on Register 9.
- Speaker Out Attenuation: Writes to SOT on Register 9.

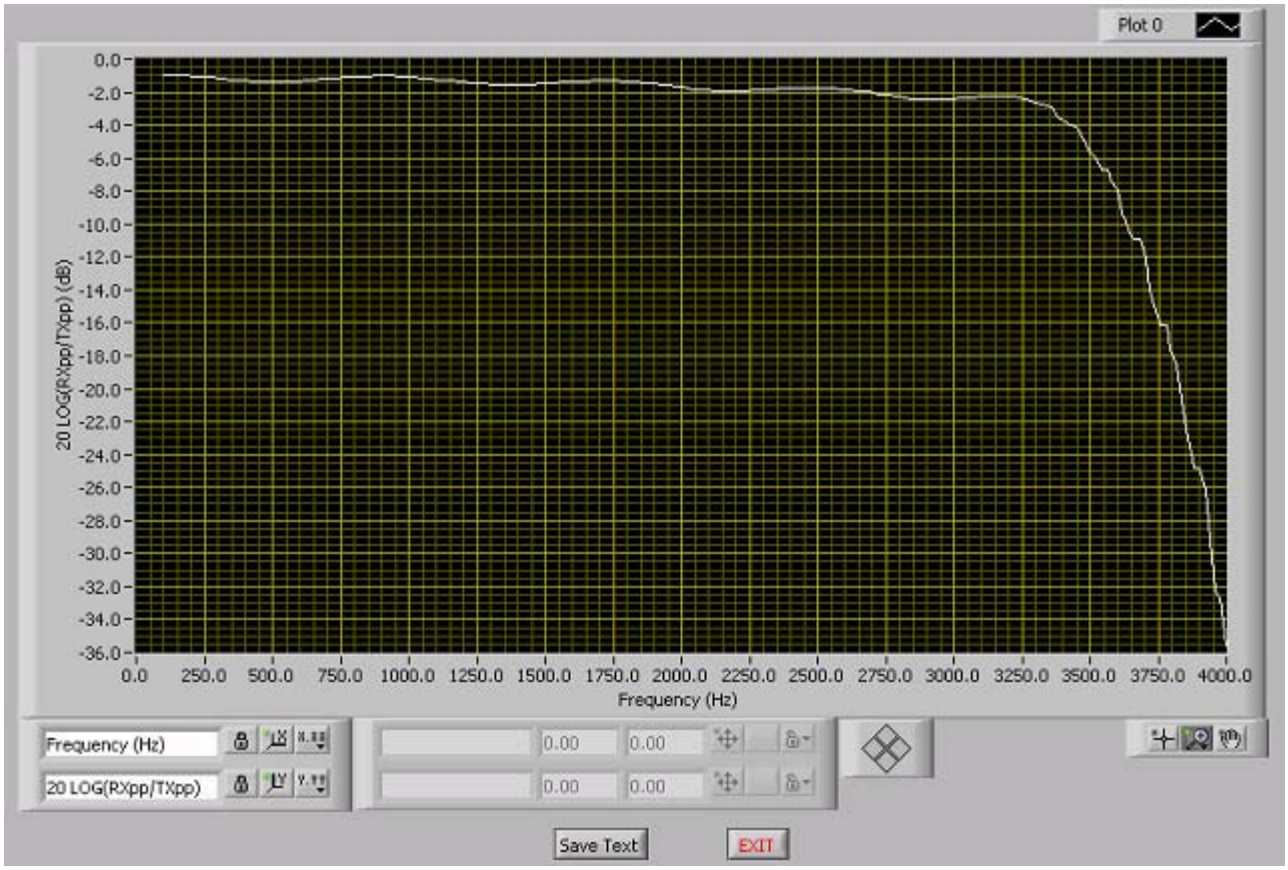


Figure 5. Transhybrid Loss

Transhybrid Loss Calculation

When “Transhybrid Loss Calculation” is selected, the Si30xxPPT-EVB software will drive a signal with different frequencies and measure the transhybrid loss based on the following equation: Transhybrid Loss = 20Log(TXpk-pk/RXpk-pk). Frequencies used to measure this start from 100 Hz to 4000 Hz in 20 Hz steps.

Ringing

This function is not availabe on the Si3000PPT-EVB.

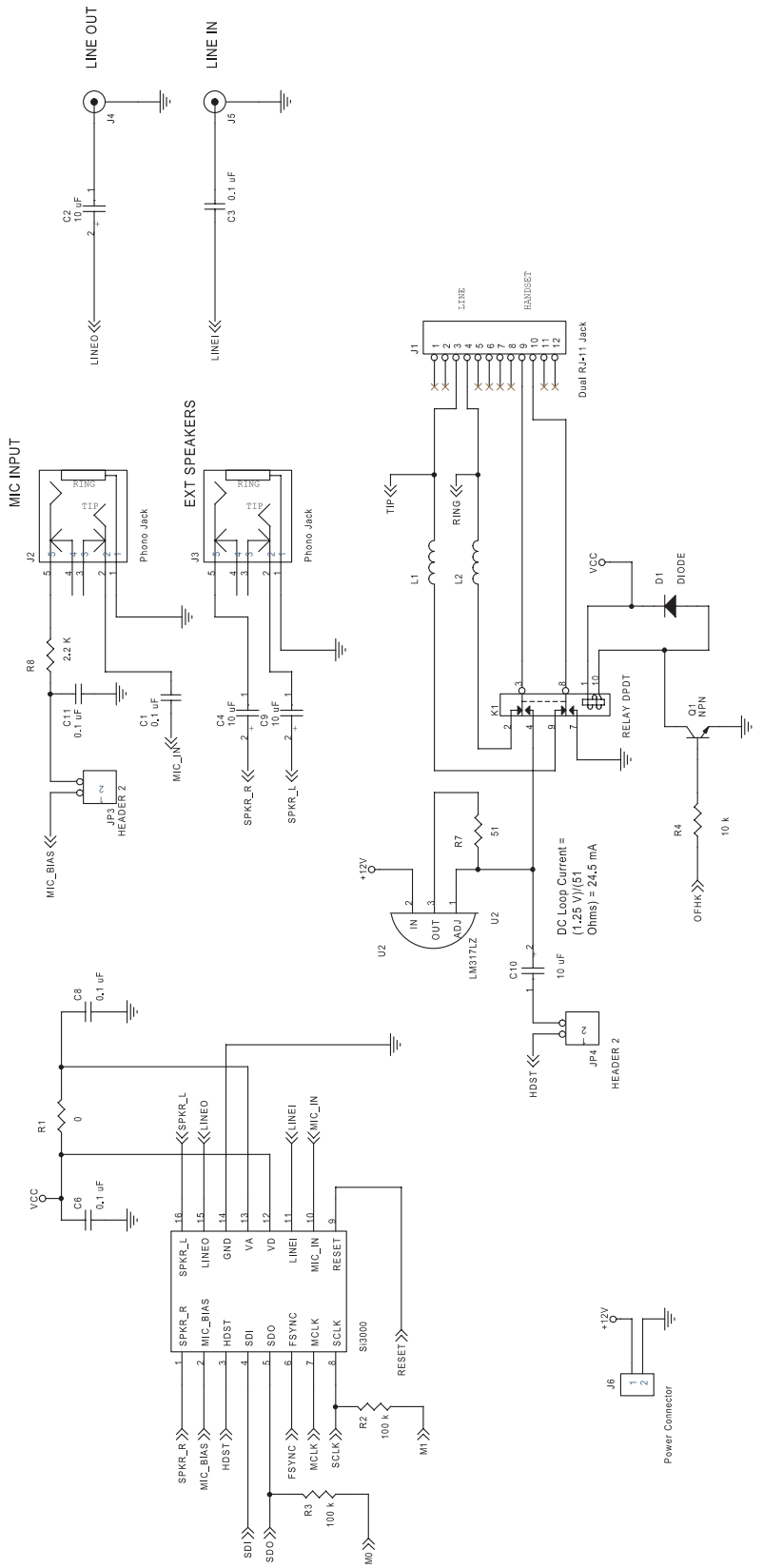


Figure 6. Si3000DC-EVB Schematic (1 of 2)

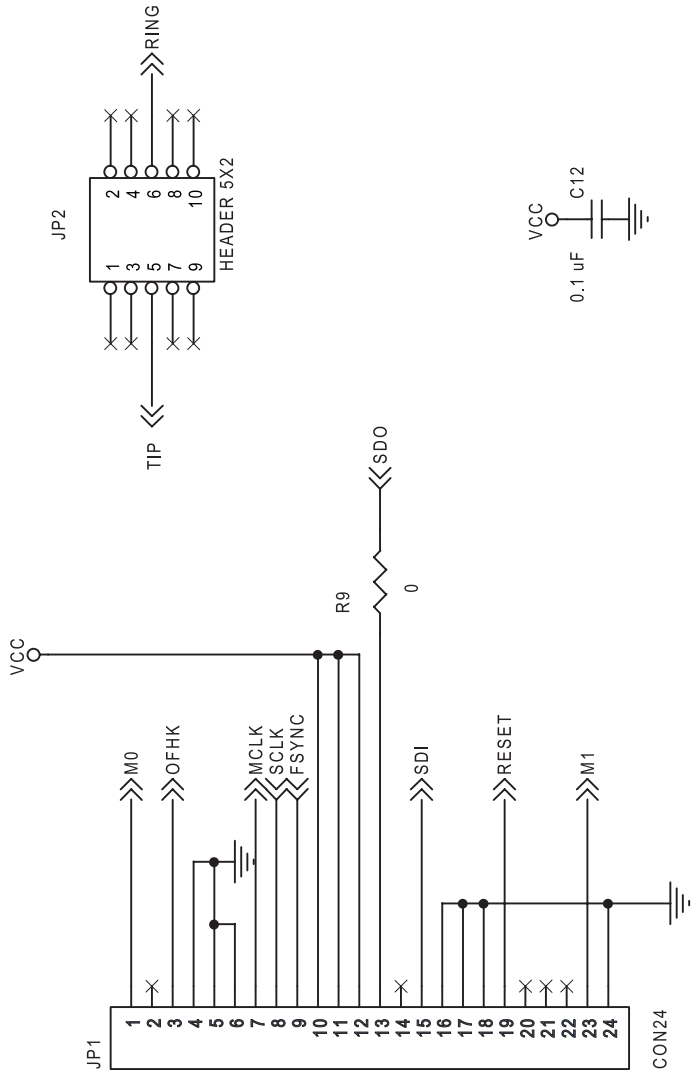
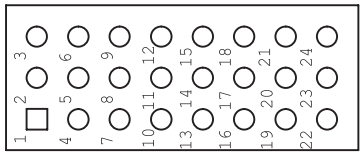


Figure 7. Si3000DC-EVB Schematic (2 of 2)



Footprint of JP1
Top View

Si3000DC-EVB Bill of Materials

Reference	Part
C1,C3,C6,C8,C11,C12	0.1 uF, 25 V, +/- 20%, 0805, X7R, C0805X7R250104-MNE, Venkel
C2,C4,C9	10 uF, 16 V, +/- 20%, case A, , TA016TCM106MAR, Venkel
C10	10 uF, 25 V, +/- 10%, case C, , TA025TCM106MCR, Venkel
D1	DIODE, , , DO-35, , 1N4148, Rectron
JP1	CON24, , , 3x8 100 mil, , SSW-108-01-T-T, Samtec
JP2	HEADER 5X2, , , 5x2 100 mil, , SSW-105-01-T-D, Samtec
JP4,JP3	HEADER 2, , , 2x1 100 mil, , 68000-402, Berg
J1	Dual RJ-11 Jack, , , RJ11x2, , MTJG-2-64-2-2-1, Adam Tech
J2,J3	Phono Jack, , , Thru-Hole, , 161-3504, Mouser
J5,J4	RCA JACK, , , thru-hole, , 16PJ097, Mouser
J6	Power Connector, , , thru-hole 2, , TSA-2, Adam Tech
K1	RELAY DPDT, 4.5V, , TQ2, , TQ2-4.5V, Aromat
L1,L2	Ferrite Bead, , , 1206, , BLM31A601S, MuRata
Q1	NPN, , , SOT-23, , CMPT2222A, Central Semiconductor
R9,R1	0, , , 0805, , CJ21-000-T, KOA
R3,R2	100 k, 1/10W, +/- 5%, 0805, , CR0805-10W-104JT, Venkel
R4	10 k, 1/4 W, +/- 5%, 1206, , CR1206-4W-103JT, Venkel
R7	51, 1/4 W, +/- 5%, 1206, , CR1206-4W-510JT, Venkel
R8	2.2 k, 1/10 W, +/- 5%, 0805, , CR0805-10W-222JT, Venkel
U1	Si3000, , , S016, , Si3000, Silicon Laboratories
U2	LM317LZ, , , TO-92, , LM317L, SGS Thompson

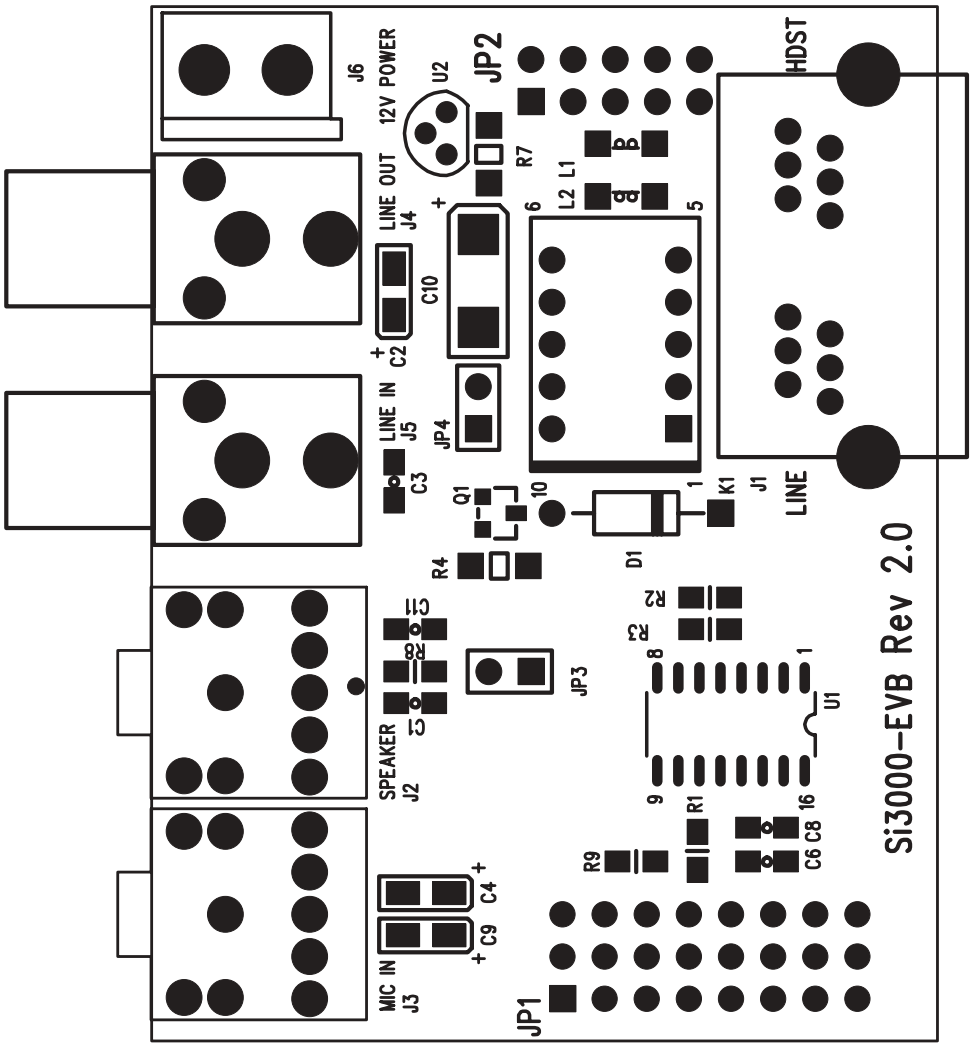


Figure 8. Si3000DC-EVB Silkscreen

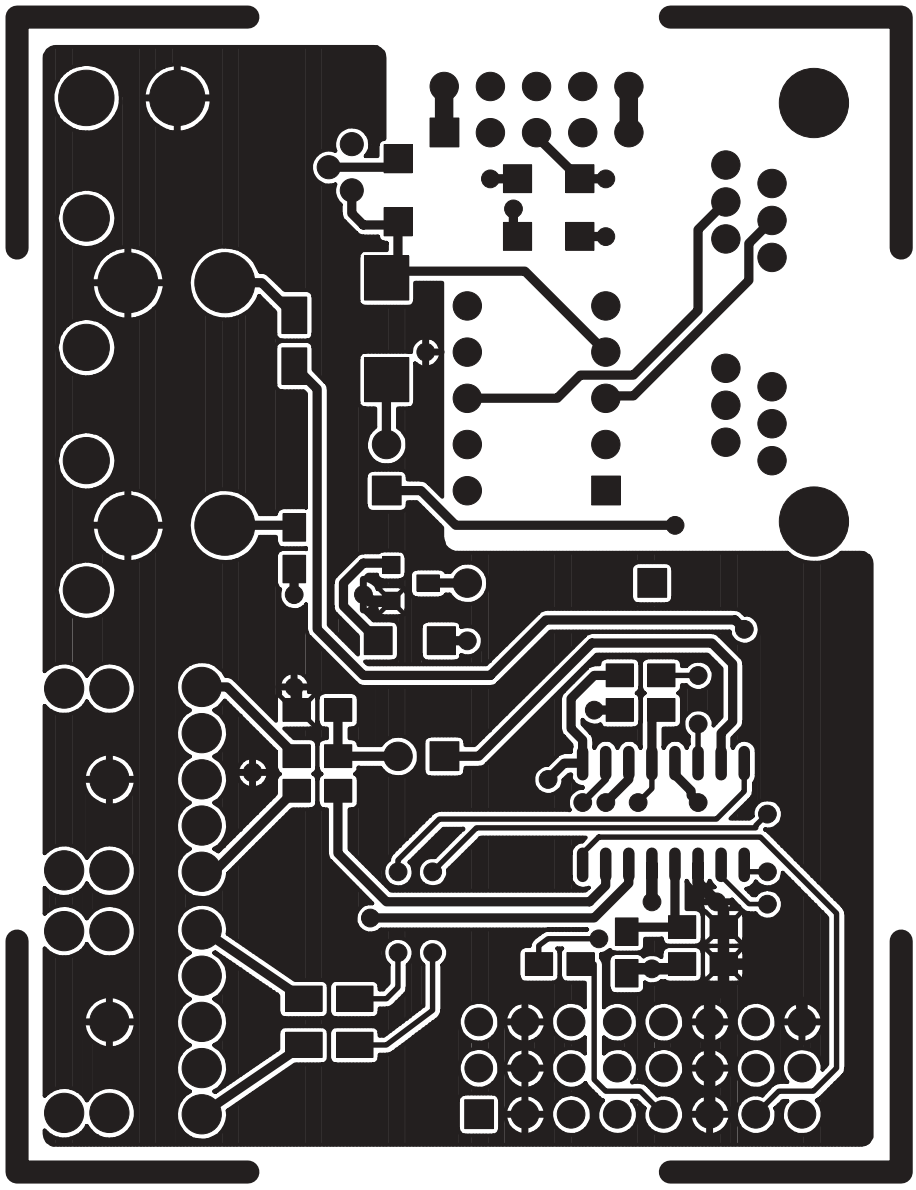


Figure 9. Si3000DC-EVB Component Side

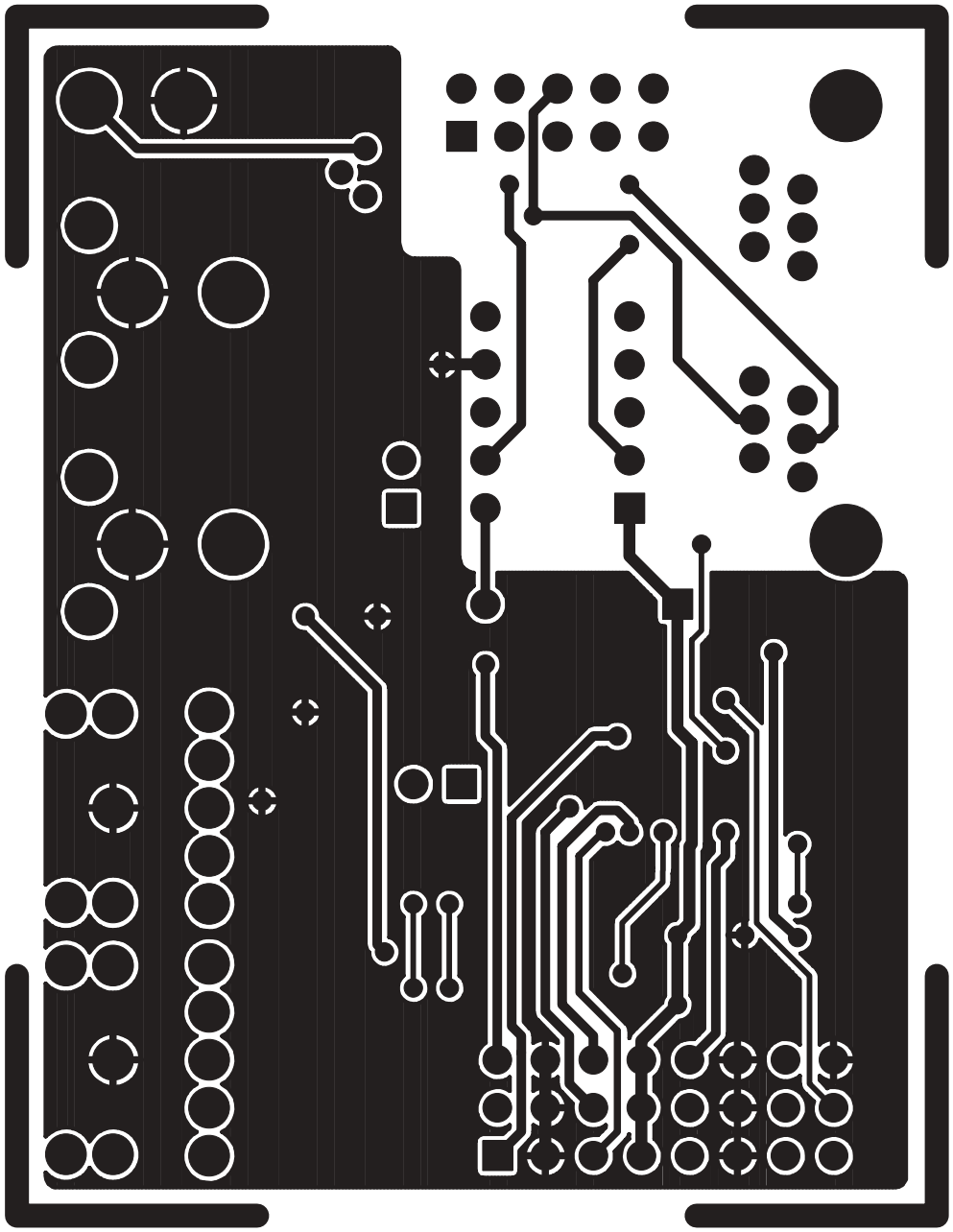


Figure 10. Si3000DC-EVB Solder Side

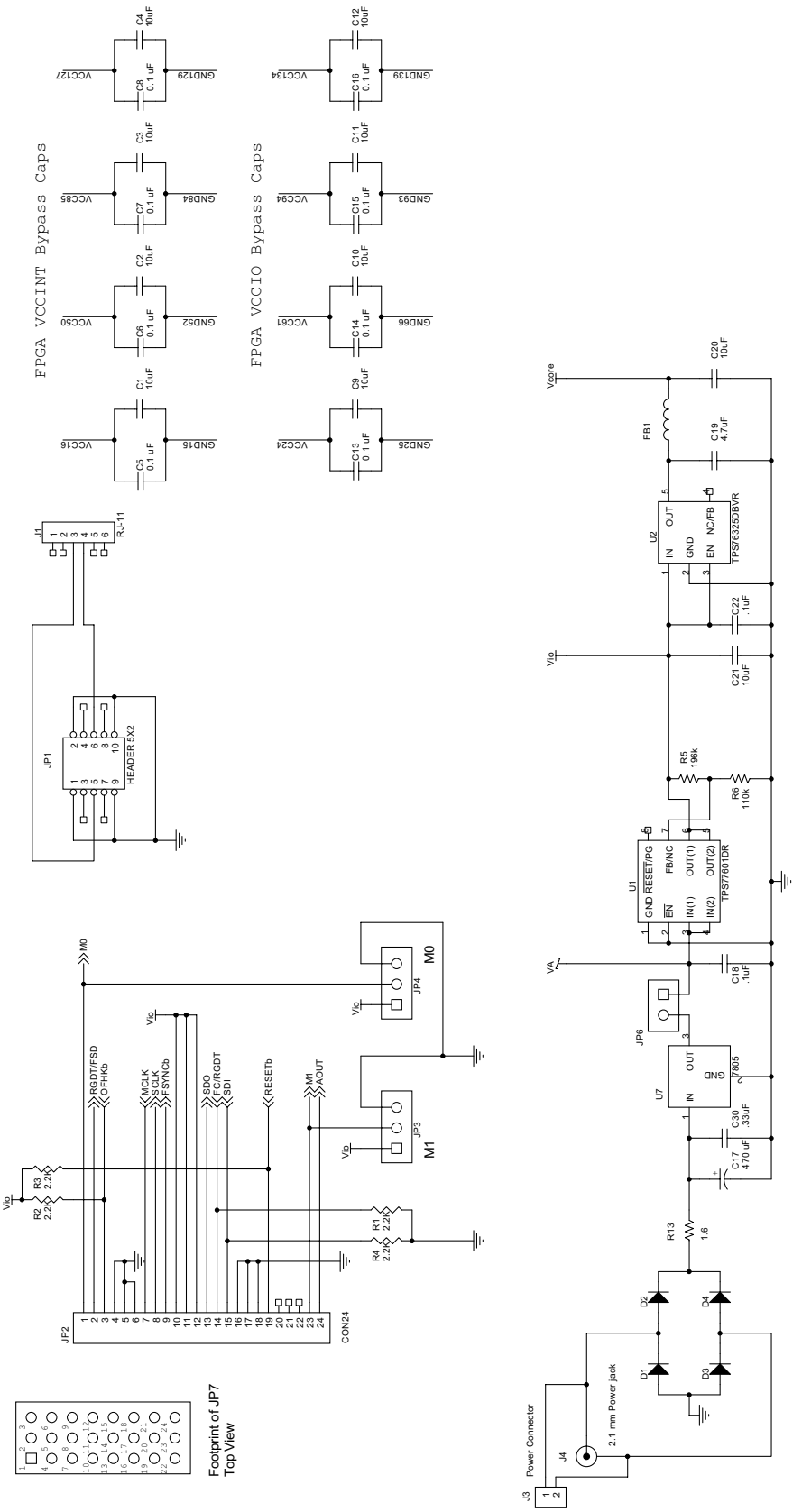


Figure 11. Si30xx Motherboard Schematic (1 of 3)

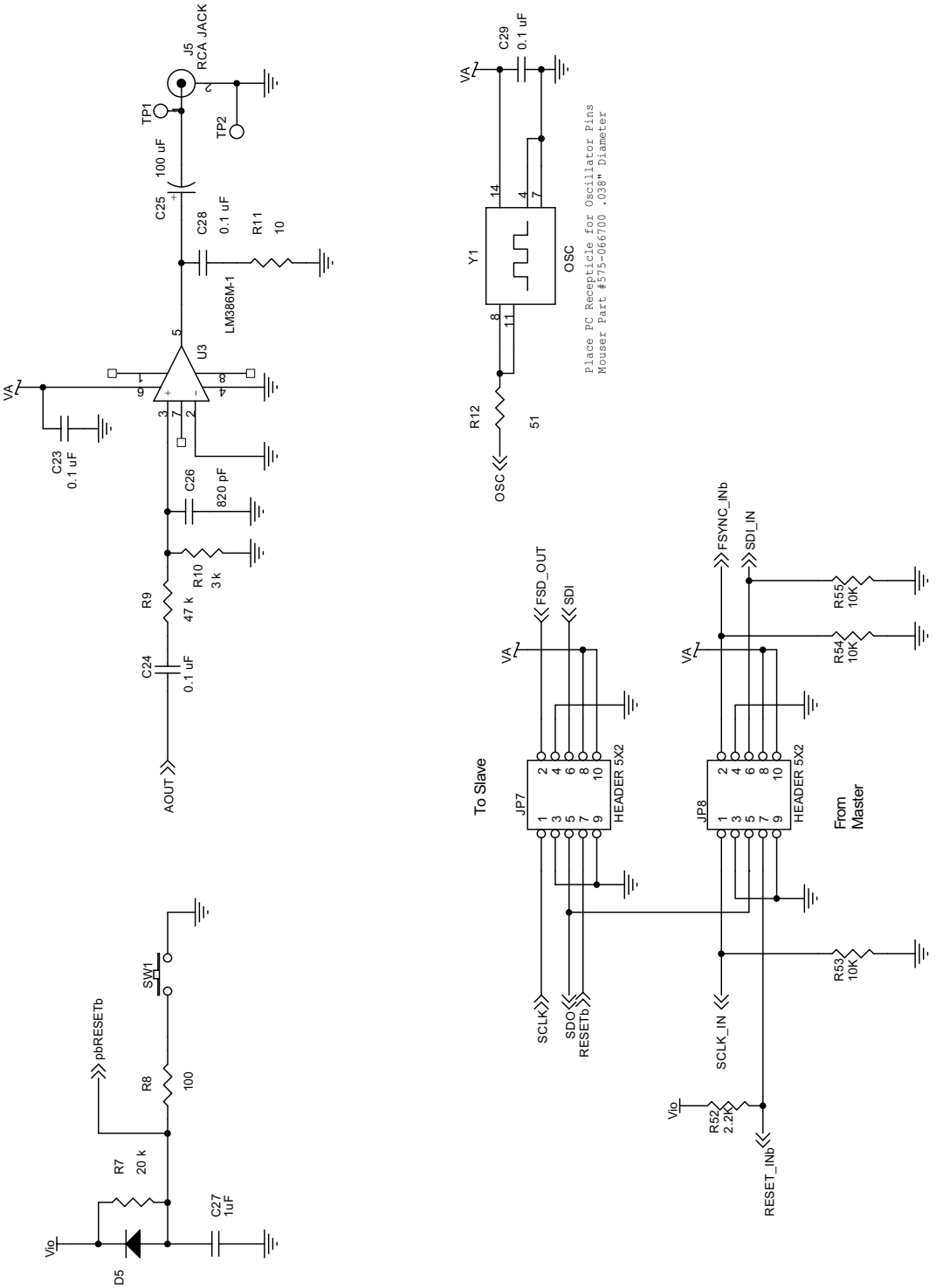


Figure 12. Si30xx Motherboard Schematic (2 of 2)

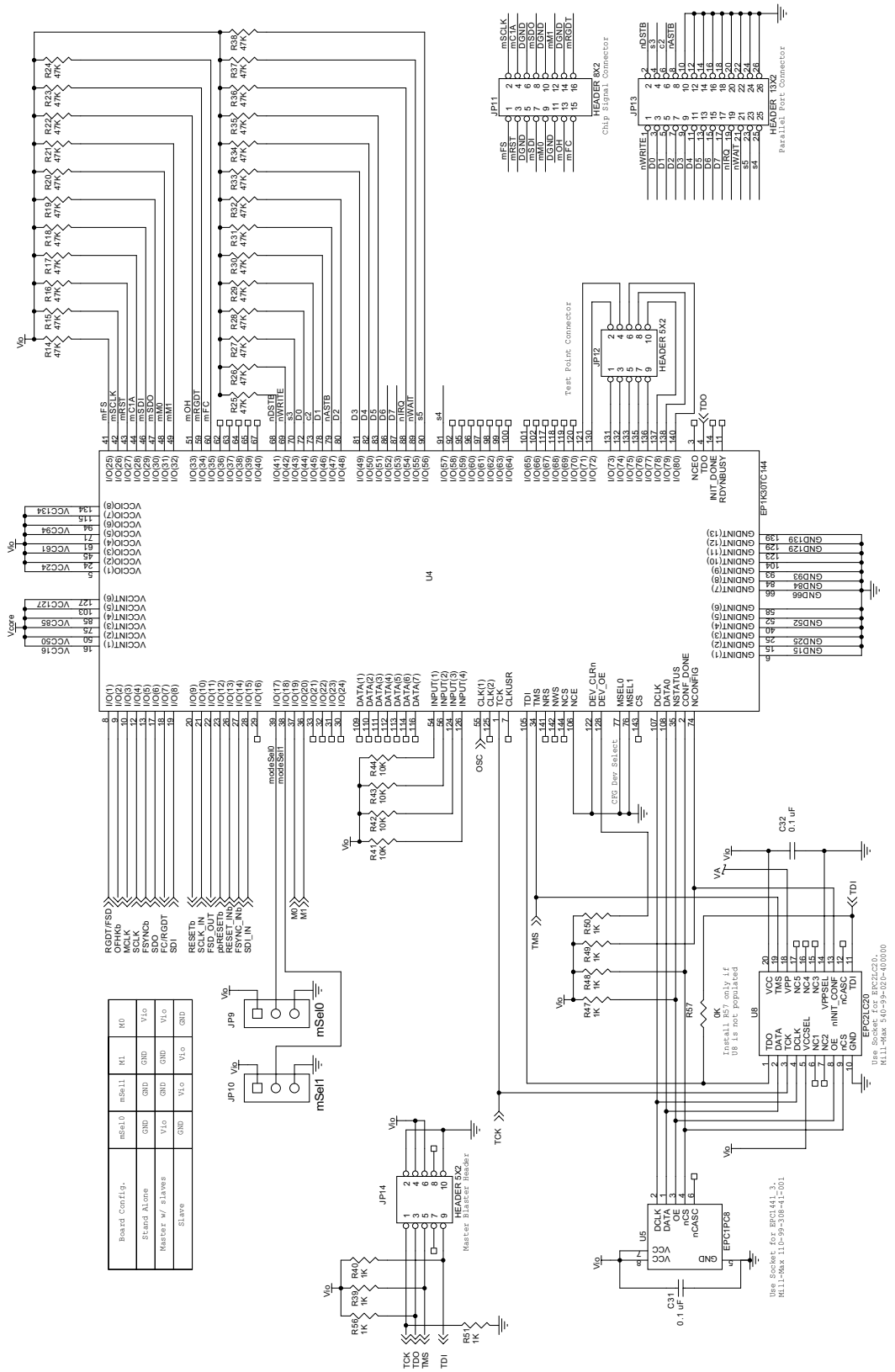


Figure 13. Si30xx Motherboard Schematic (3 of 3)

Bill of Materials: Si30xx Motherboard

Item	Qty	Reference	Part
1	10	C1,C2,C3,C4,C9,C10,C11,	10uF, 10 V, ±10%, 1206, , C1206X7R100-106KNE, Venkel
		C12,C20,C21	
2	14	C5,C6,C7,C8,C13,C14,C15, C16,C23,C24,C28,C29,C31, C32	0.1 uF, 16 V, ±10%, 0603, , C0603X7R160-104KNE, Venkel
3	1	C17	470 uF, 25 V, ±20%, radial 10x16, , UVX1E471MPA, NIC Components
4	2	C18,C22	.1uF, 25V, , 0805, , C0805X7R250-104KNE, Venkel
5	1	C19	4.7uF, 10V, +/-10%, 1206, , TDKC3216X5RA475KT, CLASSIC COMP
6	1	C25	100 uF, 16 V, ±10%, radial 6.3x11, , , TTI
7	1	C26	820 pF, 50 V, ±5%, 0805, , C0805COG500-821JNE, Venkel
8	1	C27	1uF, 10 V, ±10%, 1206, , C1206X7R100-105KNE, Venkel
9	1	C30	.33uF, 25V, , 0805, , C0805G334Z3NT, CLASSIC COMP
10	4	D1,D2,D3,D4	DIODE, 30 V, 0.5 A, SOD-123, , MBR0530T1, Motorola
11	1	D5	DIODE, 400 mA, 75 V, DO-35, , 1N4148, Diodes, Inc.
12	1	FB1	Ferrite Bead on wire, 3x1x4 (mm), , thru-hole 2, , 2743015112, Fair-Rite
13	1	JP1	HEADER 5X2, , , 5x2 100 mil, , TMM-105-01-G-D, Samtec
14	1	JP2	CON24, , , 3x8 100 mil, , TSW-108-07-G-T, Samtec
15	4	JP3,JP4,JP9,JP10	3X1 Header, , , 3x1 100 mil, , 68000-403, Berg Electronics
16	1	JP6	2X1 Header, , , 2x1 100 mil, , 517-6111TN, Mouser
17	1	JP7	HEADER 5X2, , , 10 pin thru-hole, , TSW-105-08-T-D-RA, Samtec
18	1	JP8	HEADER 5X2, , , 10 pin thru-hole, , SSW-105-02-T-D-RA, Samtec
19	1	JP11	HEADER 8X2, , , 8x2 100 mil, , ,
20	2	JP14,JP12	HEADER 5X2, , , 5x2 100 mil, , ,
21	1	JP13	HEADER 13X2, , , 13X2 100 mil, , 13x2 pin Header with Shroud, Mouser
22	1	J1	RJ-11, , , thru-hole 6, , 154-0L6641, Mouser
23	1	J3	Power Connector, , , thru-hole 2, , TSA-2, Adam Tech
24	1	J4	2.1 mm Power jack, , , thru-hole 3, , ADC-002-1, Adam Tech
25	1	J5	RCA JACK, , , thru-hole, , 16J097, Mouser
26	5	R1,R2,R3,R4,R52	2.2K, , , 0805, , CR0805-10W-222JT, Venkel
27	1	R5	196k, , , 0805, , MCHRIDEZHFX1963E, Classic Comp
28	1	R6	110k, , , 0805, , CR21-114J-T, Classic Comp
29	1	R7	20 k, 1/10 W, ±1%, 0805, , NRC10F2002TR, NIC Components
30	1	R8	100, 1/4 W, ±1%, 1206, , MCR18EZHMFX1000, Rohm
31	1	R9	47 k, 1/10 W, ±5%, 0805, , NRC10J473TR, NIC Components
32	1	R10	3 k, 1/10 W, ±5%, 0805, , NRC10J302TR, NIC Components
33	1	R11	10, 1/10 W, ±1%, 0805, , NRC10F10R0TR, NIC Components
34	1	R12	51, 1/10 W, ±5%, 0805, , CR21-510J-T, AVX
35	1	R13	1.6, , +-5%, 1206, , CR1206-8W-1R6JT, Venkel
36	25	R14,R15,R16,R17,R18,R19, R20,R21,R22,R23,R24,R25, R26,R27,R28,R29,R30,R31, R32,R33,R34,R35,R36,R37, R38	47K, , , 0603, , CR0603-16W-473JT, Venkel
37	2	R40,R39	1K, , , 0603, , CR0603-16W-1002FT, Venkel
38	7	R41,R42,R43,R44,R53,R54, R55	10K, , , 0603, , CR0603-16W-1002FT, Venkel
39	6	R47,R48,R49,R50,R51,R56	1K, , , 0603, , MCR03FZHJ102, TTI
40	1	SW1	SW PUSHBUTTON, , , thru-hole 4, , 101-0161, Mouser
41	1	TP1	Test Point, , , thru-hole, , 151-207, Mouser
42	1	TP2	Test Point, , , thru-hole, , 151-203, Mouser
43	1	U1	TPS77601DR, , , 8-Pin SOIC, , , Texas Instruments
44	1	U2	TPS76325DBVR, , , 5-Pin SOT-23, , , Texas Instruments
45	1	U3	OP-AMP, , , M, , LM386M-1, National Semi
46	1	U4	EP1K30TC144, , , TQFP-144, , EP1K30TC144-3, Altera
47	1	U7	7805, , , TO-220AB, , uA7805CKC, Texas Instruments
48	1	U5	Socket, , , DIP-8, ,110-99-308-41-001, Mill-Max
49	6	Y1	PC Recepticle, .038" Diameter, 575-06670, Mouser
50	1	R57	0K, , , 0603, , CR0603-16W-000T, Venkel
51	4	N/A	1/2" Plastic Standoff
52	4	N/A	Plastic Screw

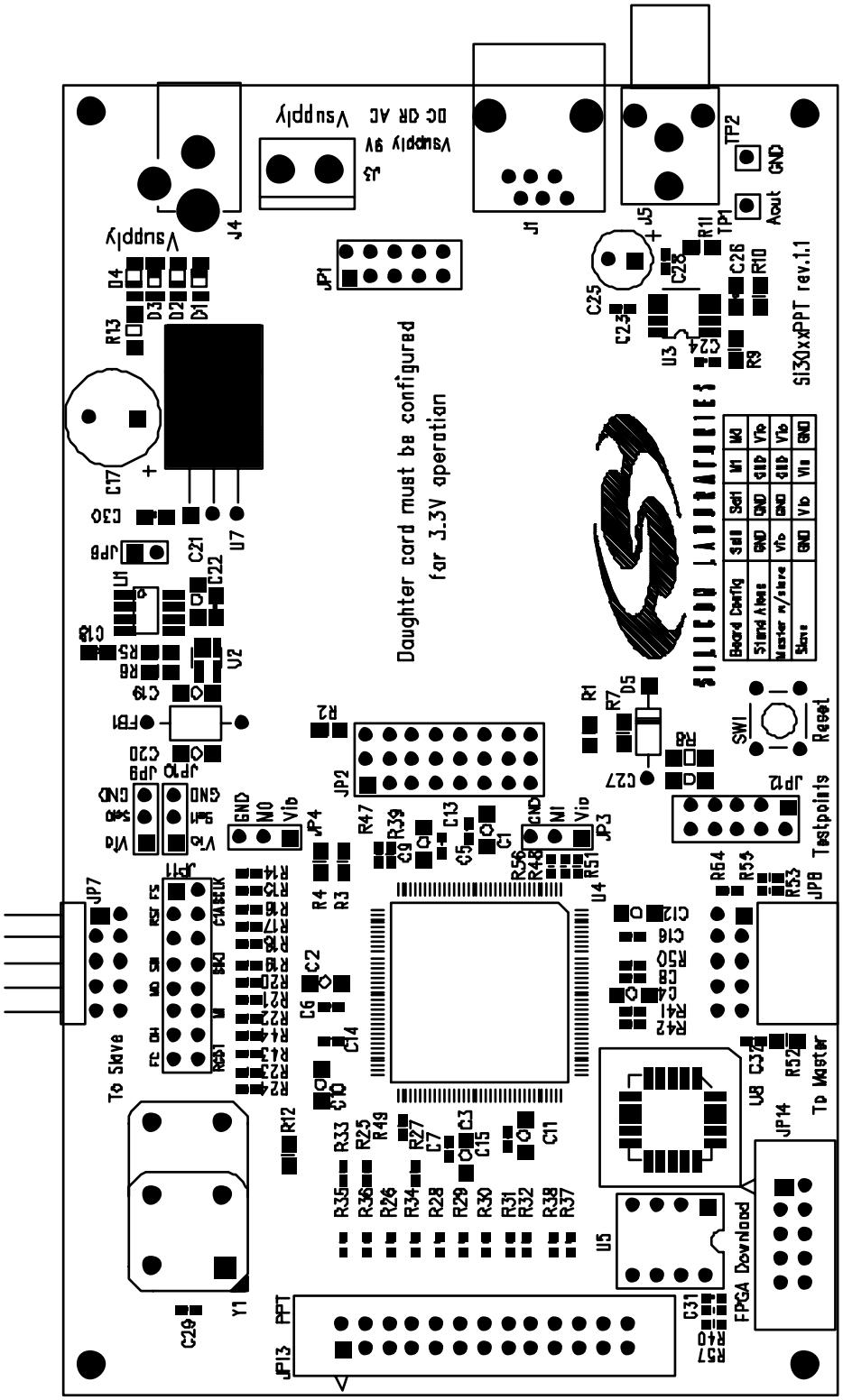


Figure 14. Si30xx Motherboard Schematic (1 of 3)

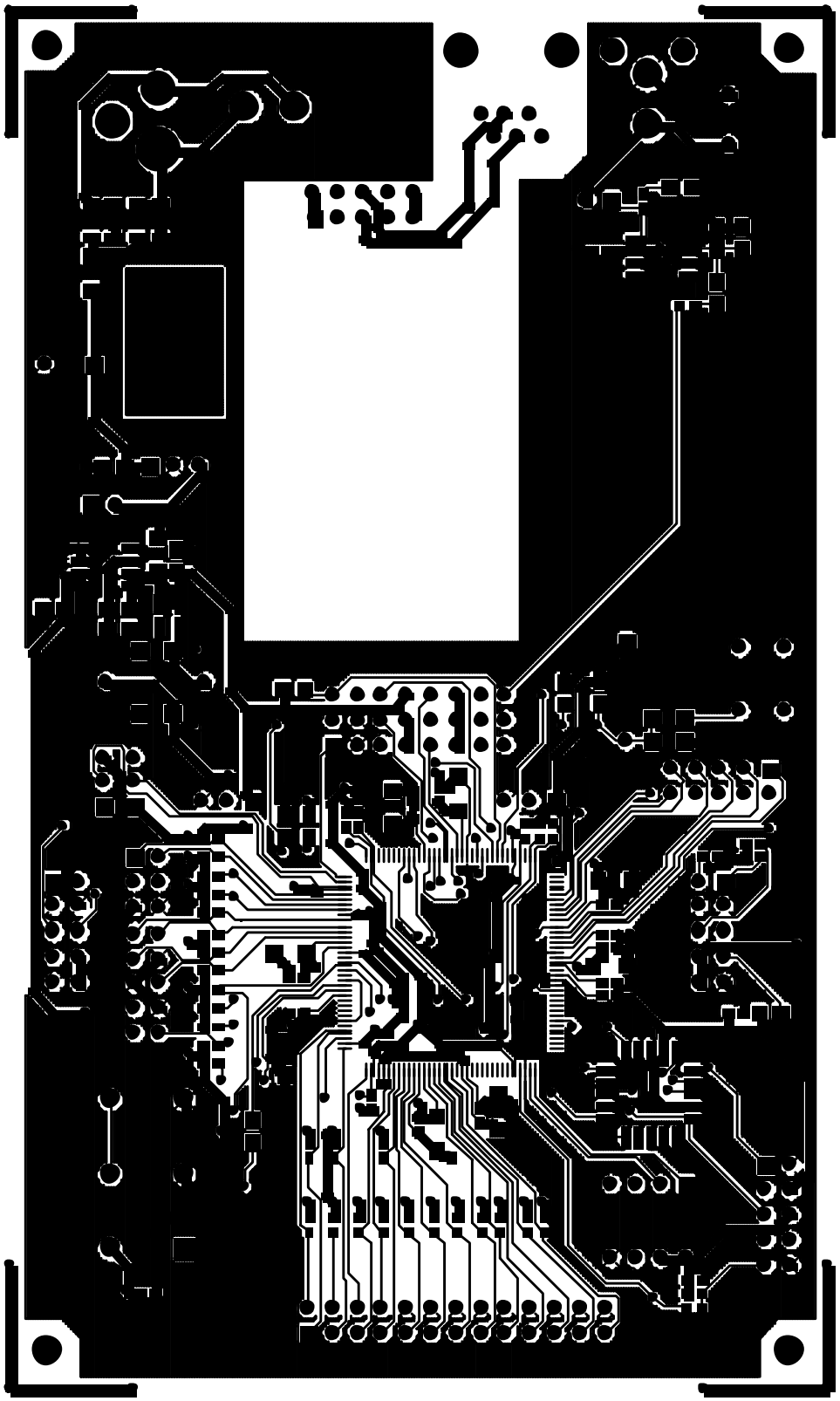


Figure 15. Si30xx Motherboard Component Layer

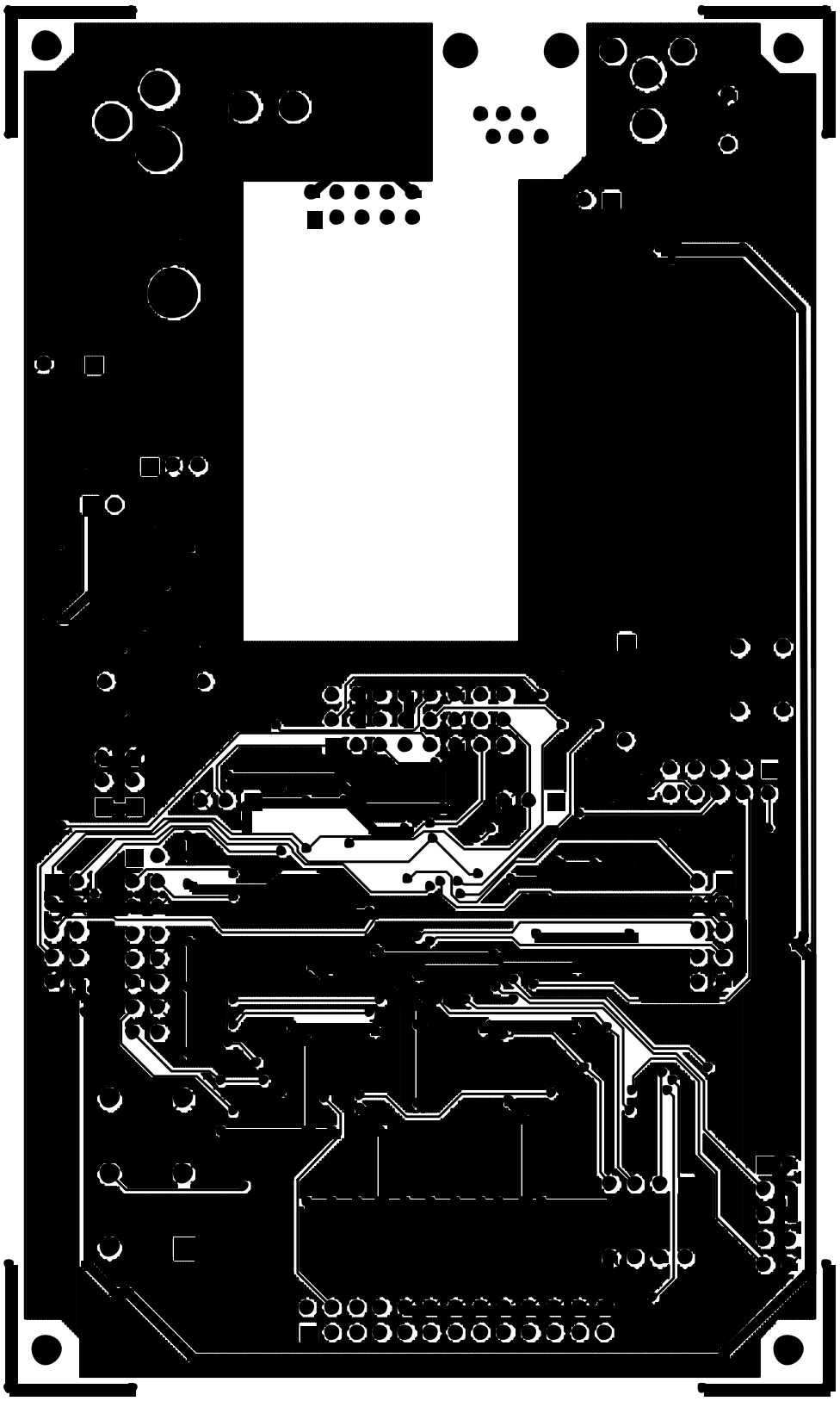


Figure 16. Si30xx Motherboard Solder Layer

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